REMARKS/ARGUMENTS

Claims 1, 2-4, 6, 8-12, 14, 16-18 and 20-24 are now pending in this application. Claims 1, 9 and 17 are independent claims. Claims 5, 7, 13, 15 and 19 have been cancelled.

Claim Rejections - 35 USC § 103(a)

Claims 1-4, 8-12, 16, 17 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, US 6,362,651 (hereinafter: Voogel) in view of Hongo et al., US 2003/0143971 (hereinafter: Hongo) and further in view of Glenn et al., US 6,962,829 (hereinafter: Glenn). (Pending Office Action, Page 2). Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, in view of Hongo, in view of Glenn, in further view of Mastro et al., US 2002/0091977 (hereinafter: Mastro). (Pending Office Action, Page 5). Claims 18 and 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, in view of Hongo, in view of Glenn, in view of Lee et al, US 6,222,212 (hereinafter: Lee). (Pending Office Action, Page 5). Applicants respectfully traverse these rejections.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that the claims rejected under this section include elements that have not been disclosed, taught or suggested by any of the references cited by the Patent Office, either alone or in combination.

Independent Claims 1, 9 and 17 each generally recite:

> "interconnect between said plurality of platform array units being pre-routed on chip."

In the present invention, the interconnect between the plurality of platform array units may be pre-routed on chip for avoiding paying for off-chip overhead (e.g. package misalignment, ESD protection, or the like). (Present Application, Paragraph 0016). The Patent Office cites Voogel as teaching the

above-referenced elements of the present invention. (Pending Office Action, Page 3). However, the Patent Office-cited portion of Voogel merely discusses a conductor which extends across scribe line space. (Voogel, Column 8, Lines 39-40). Voogel does not disclose, teach, or suggest an interconnect being pre-routed on chip as in the present invention. Nowhere in any of the cited references, either alone or in combination, are the above-referenced elements of the present invention either disclosed, taught, or suggested.

Based on the above rationale, the Patent Office has failed to make a *prima facie* case of obviousness against claims 1, 9 and 17. Thus, claims 1, 9 and 17 should be allowed over the prior art of record. Further, Claims 2-4, 6 and 8 (which depend from Claim 1), Claims 10-12, 14 and 16 (which depend from Claim 9) and Claims 18 and 20-24 (which depend from Claim 17) should also be allowed.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the pending claims is earnestly solicited.

Respectfully submitted on behalf of
LSI Logic,

By: /jeffrey m andersen/_____
Jeffrey M. Andersen
Reg. No. 52,558

Dated: February 9, 2010

Jeffrey M. Andersen
SUITER • SWANTZ PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile